The Invention Claimed is:

1. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including a selectable number of taps;

programmable circuitry for allowing a first number of taps to be specified;

processing circuitry for computing a second number of taps; and

selection circuitry for selecting one of the first and second numbers as the selectable number.

2. The circuitry defined in claim 1 wherein the selection circuitry is programmable to make its selection.

3. The circuitry defined in claim 1 wherein the processing circuitry performs an algorithm to compute the second number.

4. A digital processing system comprising:

processor circuitry;

a memory coupled to the processor circuitry; and

programmable logic device circuitry as defined in claim 1 coupled to the processor circuitry and the memory.

5. A printed circuit board on which is mounted programmable logic device circuitry as defined in claim 1.

6. The printed circuit board defined in claim 5 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device circuitry.

7. The printed circuit board defined in claim 5 further comprising:

processor circuitry mounted on the printed circuit board and coupled to the programmable logic device circuitry.

8. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including taps having a selected one of integer spacing and fractional spacing relative to the symbol rate of the data signal;

programmable circuitry for allowing a first selection between integer spacing and fractional spacing to be specified;

processing circuitry for computing a second selection between integer spacing and fractional spacing; and

selection circuitry for selecting one of the first and second selections as the selected one of integer spacing and fractional spacing.

9. The circuitry defined in claim 8 wherein the selection circuitry is programmable to make its selection.

10. The circuitry defined in claim 8 wherein the processing circuitry performs an algorithm to compute the second selection.

11. The circuitry defined in claim 8 wherein the fractional spacing is a selectable fraction of the symbol period, wherein the first selection can include a programmably specified first fraction, and wherein the second selection can include a processing-circuitry-computed second fraction.

12. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including at least one selectable coefficient value;

first processing circuitry for computing the coefficient value using a selectable starting value;

programmable circuitry for allowing a first starting value to be specified;

second processing circuitry for computing a second starting value; and

selection circuitry for selecting one of the first and second starting values as the selectable starting value.

13. The circuitry defined in claim 12 wherein the selection circuitry is programmable to make its selection.

14. The circuitry defined in claim 12 wherein the first processing circuitry performs an algorithm to compute the coefficient value.

15. The circuitry defined in claim 12 wherein the second processing circuitry performs an algorithm to compute the second starting value.

16. The circuitry defined in claim 12 further comprising:

further programmable circuitry for allowing selection between (1) operation of the first processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced.

17. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry including at least one selectable coefficient value;

processing circuitry for computing the coefficient value; and

programmable circuitry for allowing selection between (1) operation of the processing circuitry to fix on the coefficient value that produces satisfactory equalization, and (2) continued operation of the first processing circuitry to continue to possibly adapt the coefficient value even after satisfactory equalization has been produced.

18. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry responsive to an error signal;

first processing circuitry for computing a first decision directed error signal;

second processing circuitry for computing a second error using a training pattern; and

selection circuitry for selecting one of the first and second error signals as the error signal.

19. The circuitry defined in claim 18 wherein the selection circuitry is programmable to make its selection.

20. The circuitry defined in claim 18 wherein the first processing circuitry performs an algorithm to compute the first decision directed error signal.

21. The circuitry defined in claim 18 wherein the second processing circuitry performs an algorithm to compute the second error signal using a training pattern.

22. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

processing circuitry for computing an error signal using a selectable training pattern;

programmable circuitry for allowing a first training pattern to be specified;

training pattern circuitry for providing a second training pattern; and

selection circuitry for selecting one of the first and second training patterns as the selectable training pattern.

23. The circuitry defined in claim 22 wherein the selection circuitry is programmable to make its selection.

24. Programmable logic device circuitry for adaptively equalizing a received data signal comprising:

equalization implementation circuitry having at least one sampling point with a selectable location relative to a bit period of the received signal;

programmable circuitry for allowing a first location of the sampling point to be specified;

processing circuitry for computing a second location of the sampling point; and

selection circuitry for selecting one of the first and second locations as the selectable location.

25. The circuitry defined in claim 24 wherein the selection circuitry is programmable to make its selection.

26. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a number of taps to be used in equalization implementation circuitry of the device from one of a programmably specified number of taps and a computed number of taps; and

controlling the equalization implementation circuitry to operate with the number of taps selected in the selecting.

27. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a tap spacing to be used in equalization implementation circuitry of the device from one of a programmably specified tap spacing and a computed tap spacing; and

controlling the equalization implementation circuitry to operate with the tap spacing selected in the selecting.

28. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a starting value for determination of a coefficient to be used in equalization implementation circuitry of the device from one of a programmably specified starting value and a computed starting value;

using the starting value selected in the selecting to determine the coefficient; and

operating the equalization implementation circuitry using the coefficient determined in the using.

29. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting whether a coefficient to be used in equalization implementation circuitry of the device is to be determined once or on an on-going basis; and

determining the coefficient in accordance with the selecting.

30. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting an error signal from one of a decision directed error signal and an error signal produced using a training signal; and

using the error signal selected in the selecting in a determination of at least one operating parameter of equalization implementation circuitry of the device.

31. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a training pattern from one of a programmably specified training pattern and a predetermined training pattern;

determining an error signal using the training pattern selected in the selecting; and

using the error signal in a determination of at least one operating parameter of equalization implementation circuitry of the device.

32. A method of operating programmable logic device circuitry having adaptive equalization capability comprising:

selecting a sampling location to be used in equalization implementation circuitry of the device from one of a programmably specified sampling location and a computed sampling location; and

operating the equalization implementation circuitry using the sampling location selected in the selecting.